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Radiation-Hard Analog-to-Digital Converters for Space and Strategic Applications

Michael K. Gauthier
Armando Roberto V. Dantas



November 15, 1985

Prepared for

U.S. Department of the Navy
Naval Weapons Support Center

Through an agreement with

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Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

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16. Abstract <p>During the course of the Jet Propulsion Laboratory's program to study radiation-hardened analog-to-digital converters (ADCs), numerous milestones have been reached in manufacturers' awareness and technology development and transfer, as well as in user awareness of these developments.</p> <p>The testing of ADCs has also continued with twenty different ADCs from seven manufacturers, all tested for total radiation dose and three tested for neutron effects. Results from these tests are reported.</p>			
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ABSTRACT

During the course of the Jet Propulsion Laboratory's program to study radiation-hardened analog-to-digital converters (ADCs), numerous milestones have been reached in manufacturers' awareness and technology development and transfer, as well as in user awareness of these developments.

The testing of ADCs has also continued with twenty different ADCs from seven manufacturers, all tested for total radiation dose and three tested for neutron effects. Results from these tests are reported.

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SECTION 1

INTRODUCTION

Earlier surveys (late 1970s) of available analog-to-digital converters (ADCs) suitable for precision applications showed that none had the proper combination of accuracy and radiation hardness to meet space and/or strategic weapon radiation requirements.

Over the past six years there has been a dramatic increase in the number of ADCs available having the proper combination of bits of resolution, accuracy, and operational features to meet space and/or strategic weapon requirements, but the problem of radiation hardness remains. During this period, the Jet Propulsion Laboratory (JPL) has been working with the Naval Weapons Support Center (NWSC) and the Defense Nuclear Agency (DNA) to research, test, evaluate, and report on the radiation hardness of ADCs.

The objectives of the present study were to categorize and advance the radiation hardness of existing and future ADCs through system requirement, commercial device, and new ADC concept surveys; total dose and neutron testing/analysis of selected ADCs; and trade-off analysis studies and performances. Emphasis was directed at approaches that could be integrated into a monolithic chip that would have a 1 Mrad(Si) total dose and 10^{13} n/cm² neutron hardness.

Numerous milestones have been reached in ADC hardening, including raising manufacturers' awareness and improved technology development and transfer, as well as user awareness of these developments. The scanning electron microscope (SEM)^{1,2,3,4,5} at JPL was used on a few device types to assist manufacturers in hardness improvement. Increases in device hardness of up to 20 times have been achieved by this technique.

During the course of this ongoing program, JPL has radiation hardness tested twenty different ADCs from seven different manufacturers for total radiation dose and three for neutron effects. Many of the previous results have been reported on in prior reports and conferences^{6,7,8}. The latest data^{9,10} has been released this year. This paper summarizes the work completed in this area to date.

SECTION 2

MILESTONES

JPL conducted their first ADC radiation test in 1978 on the TRW-TDC 1001, 8-bit ADC. Since that first test, JPL has continued radiation testing ADCs for total radiation dose and neutron effects. The data have been published in reports^{2,4,6,10} and conference papers^{3,7} and have been included in the newly established JPL/NASA Electronic Data Bank⁹, RADATA. Along with radiation effects testing, there have been numerous other ADC related activities, in which JPL was instrumental in initiating and achieving the present status of cooperation towards the development and hardness improvements found in current ADCs.

2.1 MANUFACTURERS' AWARENESS

In 1981 all known manufacturers of ADCs were contacted for an initial survey⁸. Since that time there have been telephone calls and personal visits to key manufacturers. The overall goal was to identify sources of radiation hardened ADCs, but this also gave JPL the opportunity to inform the manufacturers of the basic requirements for space and strategic weapons, the need for radiation hardened devices, and what can be done to improve the hardness of current and future devices. Although the emphasis was on ADCs, manufacturers were encouraged to extend the radiation hardening philosophy to their entire product line. An example of this transfer is the Burr-Brown operational amplifier, OPA-111, which has been tested with Co-60 gamma rays and 2.5 MeV electrons to 10 Mrad(Si) and neutrons to $>2 \times 10^{13}$ n/cm² with little degradation noted.

2.2 IMPROVED HARDNESS

Manufacturers were encouraged to increase the hardness of their ADCs, at little or no cost, through process changes and other hardening techniques during periodic redesign, and also to incorporate as many of the hardening design techniques as practical and cost effective when designing a new device.

As an example of improving quality and radiation hardness, the scanning electron microscope (SEM)^{1,2,3,4,5} at JPL was used to locate radiation sensitive components in the Analog Device AD571 and Micro Networks MN5211 and MN5214 devices. Increases in device hardness of up to 20 times were made by the manufacturer from the design and process changes suggested by JPL.

Manufacturers now provide nine different ADCs which are known to be hard to at least 600 krad(Si). With the help of this program, Analog Devices, AMD, and Micro Networks have developed seven of the nine devices.

2.3 NEW COMPANIES

New companies, previously not ADC manufacturers, are now producing ADCs. AMD has three devices which are hard to greater than 600 krad(Si) and PMI has recently announced a new entry into the field, the ADC-910. This device has not been radiation tested but is expected to be hard to at least 500 krad(Si). This estimate is based on the "harder than average" radiation response of previously tested PMI devices.⁹ Linear Technology Corp. is also considering entering the ADC market.

2.4 TECHNOLOGY TRANSFER

ADC manufacturers in general are not radiation effects experts, although there is usually an individual or a small group within a company with a basic understanding of radiation effects. The major problem for the manufacturers has been the lack of current information on hardening techniques. In-plant meetings have been held with design, process, and management teams to bring them up-to-date with the latest radiation hardening technology. These meetings have been well received by the companies involved. To date, meetings have been held with Analog Devices, AMD, Burr-Brown, Harris, Micro Networks, and PMI.

2.5 THE RADIATION EFFECTS COMMUNITY

The JPL program has served the radiation effects community by reporting the latest ADC information through conference papers^{3,7}, technical publications^{2,8}, and published test data^{6,10}, including RADATA, the JPL/NASA Electronic Radiation Effects Data Bank⁹.

SECTION 3

CASE HISTORY: SEM ANALYSIS OF THE MICRO NETWORKS MN5214 ADC

The purpose of the scanning electron microscope (SEM) analysis was to locate the sensitive areas which caused the Micro Networks MN5214, a hybrid, 12-bit ADC, to show a greater radiation susceptibility than other devices of the same type.

3.1 DISCOVERY OF THE PROBLEM

JPL purchased two ADCs, MN5211 and MN5214, from Micro Networks for use on the Galileo spacecraft program. The devices are similar except for the input operating range. In fact, the whole MN5210 family of ADCs is so functionally similar that the initial radiation tests for these devices were conducted on the MN5216. This method was used because of the lack of availability of MN5211 and MN5214 devices and their high unit cost. The tests indicated the device was functional to at least 150 krad(Si).

When the initial flight devices were received by JPL, a total dose radiation test was conducted on two samples of each. The devices were irradiated at Boeing Radiation Effects Laboratory (BREL) with 2.2 MeV electrons from their Dynamitron. The MN5211 remained functional to at least 600 krad(Si) while the MN5214 failed at 30 krad(Si). The specification limit for these devices was 150 krad(Si).

3.2 ANALYSIS

Both device types were delidded and photographed for a visual comparison. The factory was contacted regarding the "as-built" information. It was learned that there were minor differences within each hybrid which was verified with the photographs (Fig. 1). One of the differences noted was the operational amplifier (chip #3), which was a 1556. Micro Networks stated that the MN5211 contained a Motorola MC1556 while the MN5214 contained a Raytheon RM1556.

3.2.1 SEM Testing

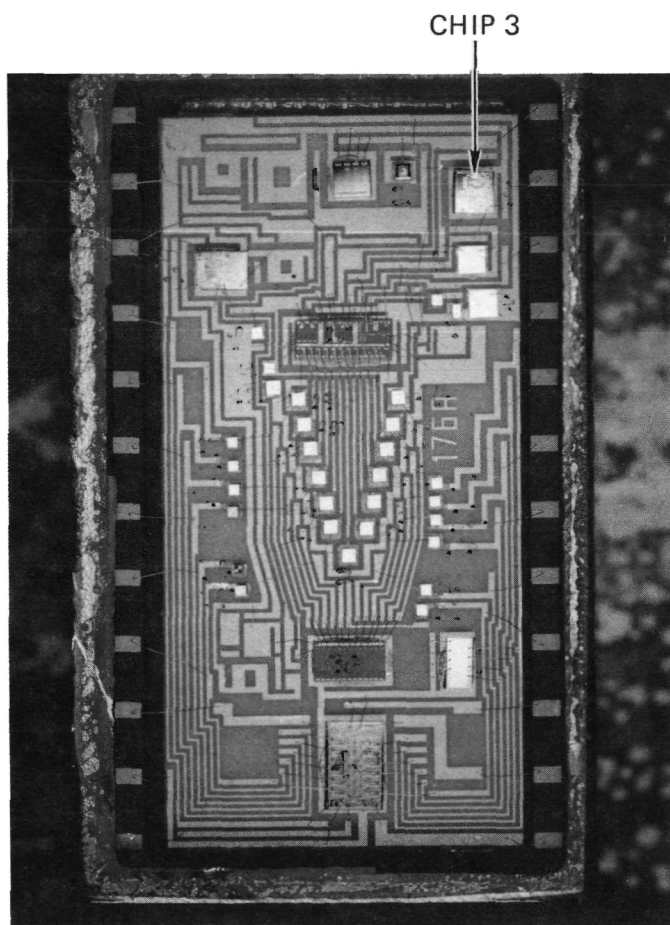
Using a previously developed technique^{1,2,3,4,5}, 30 keV electrons from a Cambridge Mark II SEM were used to irradiate samples of the MN5211 and MN5214 while under electrical bias. The flux rates were between 1.5 and 2.9 krad(Si)/sec*. Each chip in the hybrid was selectively irradiated, with

$$*\text{Flux Rate [rad(Si)/sec]} = \frac{K(E) \times I}{1.6 \times 10^{-19} \text{ coulombs} \times A}$$

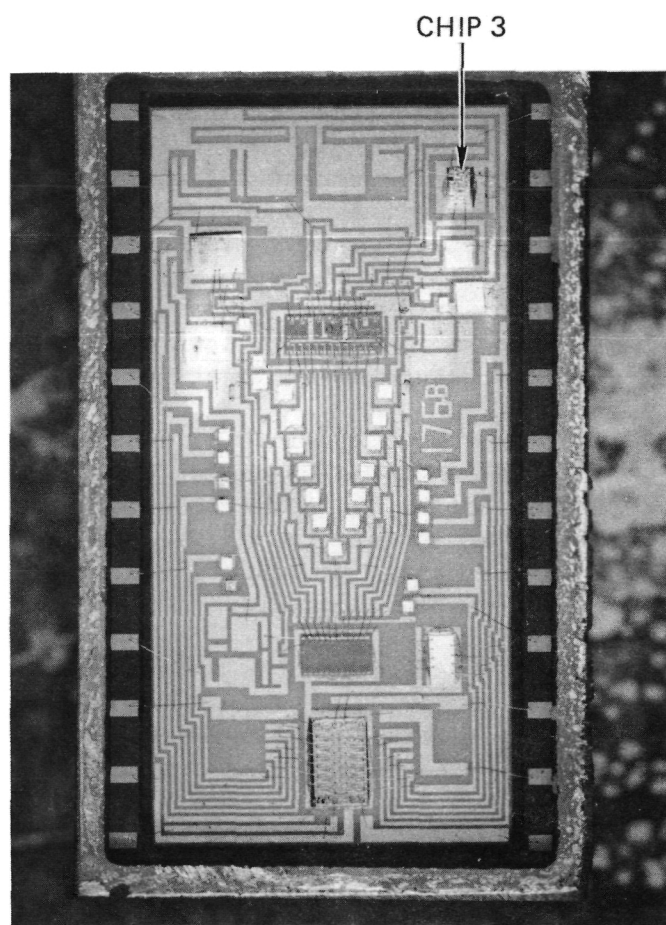
$$K(E) = \frac{dE}{dx} = 1.2 \times 10^{-7} \text{ MeV/gm-cm}^2 \text{ (for 30 keV electrons)}$$

A = area irradiated in cm², I = electron current in Amperes,
rad = 100 ergs/gm, K = an energy dependent absorption constant

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S/N 0039 Log 3720 MN5211/90227
Did not fail under irradiation.
Chip 3 is Motorola 1556.



S/N 0018 Log 3720 MN5214/90228
Failed under irradiation.
Chip 3 is Raytheon 1556.

Figure 1. Macro photographs of the MN5211 and MN5214 ADCs

the suspected chip exposed last. Electrical parameter measurements were made on the devices after each exposure. After a total dose of 30 krad(Si) neither hybrid indicated any sign of degradation.

A second irradiation of 60 krad(Si), or 90 krad(Si) total dose, was performed on each hybrid. The MN5211 indicated no sign of degradation; however, the MN5214 indicated a catastrophic failure upon exposure of the last chip, the operational amplifier (chip #3).

3.2.2 SEM Test Results

The susceptible operational amplifier on the MN5214 was manufactured by Raytheon and the unaffected counterpart on the MN5211 was manufactured by Motorola. Other differences between the two hybrids, that were noted from a study of the photographs, did not affect the performance of the ADC under the SEM irradiation of 90 krad(Si) total dose. Barring susceptibility of the other (different) chips on the MN5214, it was concluded that replacement of the Raytheon operational amplifier with a Motorola version would alleviate the sensitivity problem.

3.2.3 Total Dose Testing

Micro Networks agreed to rework the existing MN5214 devices, replacing the radiation sensitive Raytheon operational amplifier with the harder Motorola chip. Upon delivery of the rebuilt devices (now identified as MN90228, special build) two sample lots were tested. At 150 krad(Si) all devices indicated linear degradation similar to the MN5211. Measurements were then taken after 300 krad(Si) and 600 krad(Si). In the two device types tested, one type showed failures at 600 krad(Si). The other devices, although highly degraded, remained functional.

3.3 RESULTS

The rebuilt MN90228 devices meet the Galileo flight requirements.

Another result is that we have learned the following:

- (1) The SEM as a diagnostic tool has been shown to be a highly reproducible method of locating sensitive areas on integrated circuits;
- (2) The devices tested must be from the same lot as those used in the system;
- (3) There can be large variations in radiation hardness between hybrid devices of the same type;
- (4) Each component used to build hybrid devices requires a radiation hardness analysis, and in some cases actual testing; and
- (5) The same type of component made by different manufacturers can vary widely in radiation hardness.

SECTION 4

RECENT ADC TESTS

Since the publication of JPL's first ADC report⁸ in December 1982, there have been thirteen additional ADCs tested for total dose, three of which were also tested for neutron effects. A total of five companies' devices are represented in JPL's recent ADC test results, listed in Table 1. Brief descriptions of the devices follow. This information largely has been taken from the manufacturers' product literature.

4.1 AD573, ANALOG DEVICES, INC.¹¹

The AD573 is a complete 10-bit, successive approximation ADC consisting of a DAC voltage reference, clock, comparator, successive approximation register (SAR), and three-state output buffers. All components are fabricated to perform a fully accurate 10-bit conversion in 15 microseconds.

Operating on supplies of +5 V and -12 V to -15 V, the AD573 will accept analog inputs of 0 to +10 V, unipolar, or -5 V to +5 V, bipolar. A positive pulse on the CONVERT line initiates the 15-microsecond conversion cycle, and DATA READY indicates completion of the conversion. HIGH BYTE ENABLE (HBE) and LOW BYTE ENABLE (LBE) control three-state output buffers. The AD573 interfaces to most popular 8- or 16-bit microprocessors without external buffers or peripheral interface adapters. The 10 output data bits can be read as a 10-bit word or as 8- and 12-bit words.

The AD573S guarantees 10-bit accuracy and no missing codes from -55°C to +125°C. The AD573SD/883B is screened in accordance with the Class B requirements of MIL-STD-883, Method 5004, and is offered in a 20-pin hermetically sealed ceramic DIP.

4.2 AD574A, ANALOG DEVICES, INC.¹¹

The AD574A is a complete 12-bit, successive approximation ADC with tri-state output buffer circuitry for direct interface to an 8-, 12- or 16-bit microprocessor bus. The AD574A design is implemented with two LSI chips each containing both analog and digital circuitry, resulting in the maximum performance and flexibility at the lowest cost.

One chip is the high performance AD565A 12-bit DAC and voltage reference. It contains the high speed current output switching circuitry, laser-trimmed thin film resistor network, low temperature coefficient buried zener reference and the precision input scaling and bipolar offset resistors. The second chip uses the LCI (linear-compatible integrated injection logic) process to provide the low-power I²L, successive approximation register, converter control circuitry, clock, bus interface, and high performance latching comparator. The precision, low-drift comparator is adjusted for initial input-offset error at the wafer stage by the "Zener-zap" technique, which trims the comparator input stage to 1/10 LSB typical error.

Table 1. Radiation hard ADCs

Part No.	Mfg	Bits	Power, mW	Speed, μ sec	Total Dose, krad(Si)	Neutron, n/cm ²	Process	Comments
AM6108	AMD	8	600	0.5	600	>10 ¹³	Bipolar	Tri-State Output
AM6148	AMD	8	600	0.9	600	-	Bipolar	Similar to AM6108
AD573	ADI	10	350	15	30	-	I ² L	Similar to AD571, μ P Bus Interface
AD574	ADI	12	400	25	30	<3x10 ¹²	I ² L	2 Chip Hybrid
AD574 MONO	ADI	12	<400	<25	>1000	-	Bipolar	Monolithic
AM6112	AMD	12	600	3.0	600	>10 ¹³	Bipolar	Tri-State Output
HI-574A	Harris	12	500	25	10	-	CMOS/Bipolar	Similar to AD574A
HI-674A	Harris	12	500	12	10	-	CMOS/Bipolar	Faster Version of the HI574A
MN5211	Micro Networks	12	915	13	> 600	-	Bipolar	TTL Output
MN5214	"	12	915	13	30	-	Bipolar	TTL Output
MN90228	"	12	915	13	> 600	-	Bipolar	Similar to MN5214
MP574A	Micro Power	12	600	25	50	-	CMOS/Bipolar	Similar to AD574A
MN5290	Micro Networks	16	830	40	>1000	-	Bipolar	Serial and Parallel Outputs

The AD574A is available in six different grades. The AD574AJ, AK, and AL grades are specified for operation over the 0 to + 70°C temperature range. The AD574AS, AT, and AU are specified for the -55°C to +125°C range. All grades are packaged in a low-profile, 0.600-inch wide, 28-pin hermetically sealed ceramic DIP.

4.3 AD574-MONO, ANALOG DEVICES, INC.¹²

The AD574-MONO is a new monolithic design of the standard 12-bit successive approximation ADC with tri-state output buffer circuitry for direct interface to an 8-, 12- or 16-bit microprocessor bus. The AD574-MONO design is implemented with a single LSI chip containing both analog and digital circuitry, resulting in performance and flexibility at the lowest cost.

The operational description is the same as the AD574A, as described above in paragraph 4.2.

4.4 AM6108, ADVANCED MICRO DEVICES, INC.¹³

The AM6108 is a monolithic, high-speed, microprocessor-compatible ADC that converts analog input signals into an 8-bit digital output code in less than 1 microsecond. The digital output code is selected by the user as either a two's complement or offset binary. Due to the high-speed conversion, "WAIT" states are no longer necessary for most microprocessor-based data conversion/acquisition systems or instrumentation.

The AM6108 consists of an 8-bit DAC, high-speed comparator, SAR, 2.5 V reference and control logic. The 2.5 V reference is implemented utilizing the band-gap voltage of silicon. The digital outputs are tri-state buffers with the standard TTL levels for logic 1 and 0, which allows the user to conveniently interface with the microprocessor data bus. Internal scaling resistors enable the AM6108 to handle input signal ranges of 0 to +5 V, and 0 to +10 V with the device operating at ± 5 V supplies.

The AM6108DM guarantees 8-bit accuracy and no missing codes from -55°C to +125°C and is offered in a 28 pin hermetic package.

4.5 AM6112, ADVANCED MICRO DEVICES, INC.¹⁴

The AM6112 is the first monolithic microprocessor-compatible, 12-bit high-speed ADC. The AM6112 high-speed ADC contains a precision reference, DAC, comparator, SAR, scale resistors, tri-state output buffers, and comprehensive control logic, enabling the device to be interfaced with a variety of microprocessors. The AM6112 is capable of completing a 12-bit conversion in under three microseconds and can operate with input voltage ranges of 0 to +10 V, 0 to +5 V, and ± 5 V without external components.

The AM6112 has four modes of operation, two for microprocessors, one for DMA, and a "stand-alone" mode. These modes are software programmable, except for the stand-alone, which is pin selectable. The AM6112 is easily interfaced with 8- and 16-bit microprocessors. It is guaranteed monotonic with no missing codes over the full operating range of -55°C to +125°C, and is packaged in a 24-pin hermetic DIP.

4.6 AM6148, ADVANCED MICRO DEVICES, INC.¹⁵

The AM6148 is a microprocessor-compatible ADC, and is the first monolithic high-speed 8-bit ADC to include a precision reference, DAC, comparator, SAR, scale resistors, tri-state output buffers, and control logic. The AM6148 is capable of completing an 8-bit conversion in under one microsecond and can operate with input voltage ranges of 0 to +10 V, 0 to +5 V, and ± 5 V without external components. With appropriate external resistors, the user can program the device to operate on other input signal ranges (2 or 3 precision resistors are required). Full 8-bit performance is guaranteed over temperature. The device has tri-state outputs for bus compatibility and 2 status outputs - one a standard TTL signal and the other available as a status output on the data bus.

The AM6148 is useful in microprocessor-based systems or can be used in a stand-alone mode. The conversion time is short enough to allow most microprocessors to accept data immediately after requesting a conversion. The AM6148 is the same as the AM6108 except some of the pins, including data status, positive reference, and the inventing comparator input, have been deleted. The AM6148 is guaranteed for 8-bit accuracy and no missing codes from -55°C to $+125^{\circ}\text{C}$ and is offered in a 24-pin hermetic package.

4.7 HI-574A, HARRIS CORPORATION¹⁶

The HI-574A is a complete 12-bit ADC including a +10 V reference, clock, tri-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28-pin package. The bipolar analog die features the Harris dielectric isolation process, which provides enhanced AC performance and freedom from latch-up.

The voltage comparator features high power supply ripple rejection plus a high-speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. Noise has been reduced by a factor of 2 by using current instead of voltage for transmission of signals between the analog and digital ICs, and the clock oscillator is current-controlled for excellent temperature stability. The oscillator is trimmed for a nominal conversion time of $20 \pm 1 \mu\text{s}$.

The HI-574A offers standard unipolar and bipolar input ranges, and is laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient. Power requirements are +5 V and ± 12 V to ± 15 V, with typical dissipation of 515 mW. All models are packaged in a 28-pin side-brazed, ceramic DIP. MIL-STD-883 Method 5004, Class B screening is available.

4.8 HI-674A, HARRIS CORPORATION¹⁷

The HI-674A is a complete 12-bit ADC including a +10 V reference, clock, tri-state outputs and a digital interface for microprocessor control. This ADC is a higher speed (nominal conversion time of $12 \pm \mu\text{s}$) version of the HI-574A, as described above in paragraph 4.7.

4.9 MP574, MICROPOWER SYSTEMS, INC.¹⁸

The MP574 is a complete 12-bit, successive approximation ADC with tri-state output buffers for direct interface to 8- or 16-bit microprocessor buses. The MP574 is implemented with advanced bipolar and CMOS LSI chips resulting in maximum performance at lowest cost. The SAR, 12-bit decoded D/A, control logic, switches and buffers are fabricated using CMOS processing for lowest power, while a unique comparator, reference and required amplifiers are fabricated using linear bipolar processes for maximum speed and reduced offset and drift over temperature.

The MP574 is offered in a 28 pin hermetically sealed package for use over a wide temperature range and for MIL-STD-883 requirements. The lower cost proprietary commercial package is offered for applications not requiring the wider temperature exposure.

The MP574 is available in 6 product grades. The MP574J, K and L are specified for a temperature range of 0°C to +70°C while the MP574S, T and U are specified over the MIL temperature range -55°C to +125°C. The MP574 is also available with full MIL-STD-883 screening, processed in accordance with Method 5008.

4.10 MN5211, MICRO NETWORKS COMPANY¹⁹

The MN5211 device is a high-speed, 12-bit, successive approximation ADC in the industry standard 24 pin dual-in-line package. Conversion time is 13 μ sec and all specifications are met with a 1-MHz clock. Functional laser trimming of the highly stable thin-film resistor networks results in adjustment-free devices that are extremely accurate and highly stable. Zero error, for example, is guaranteed to be better than $\pm 0.025\%$ FSR at +25°C and better than $\pm 0.05\%$ FSR over the entire operating temperature range. All units are fully specified and 100% tested for linearity and accuracy at their operating temperature extremes as well as at room temperature.

The input voltage range is -5 V to +5 V and has an internal 6.3 V reference. The linearity is $\pm 1/2$ LSB and no missing codes are guaranteed over the entire operating temperature range.

The MN5211 may be procured for operation over the full -55°C to +125°C military temperature range or the 0°C to +70°C commercial temperature range. In addition, high-reliability processing, screening, and qualification according to Method 5008 of MIL-STD-883 are available.

4.11 MN5214, MICRO NETWORKS COMPANY¹⁹

The MN5214 device is a high-speed, 12-bit, successive approximation ADC in the industry standard 24-pin dual-in-line packages. Conversion time is 13 μ sec and all specifications are met with a 1 MHz clock. This ADC is similar to the MN5211, as described above in paragraph 4.10, except it uses a -10.000 V external reference for improved overall accuracy.

4.12 MN5290, MICRO NETWORKS COMPANY¹⁹

The MN5290 is a high-performance, dual-in-line package, 16-bit ADC specifically designed for use in military/aerospace and industrial applications that demand fully guaranteed high-resolution performance over extended operating temperature ranges. These successive approximation ADCs exploit the stability and tracking advantages of both SiCr and NiCr thin-film resistor technologies. Fully assembled devices are functionally laser trimmed before and after a proprietary resistor stabilization process for temperature stability. There are 4 models in the MN5290 family. All operate from -55°C to +125°C, and each guarantees no missing codes.

This device is complete with internal clock and reference and has 6 user-selectable input ranges. Output data is straight binary coded for unipolar input ranges and offset binary coded for bipolar input ranges and is available in either serial or parallel format. Conversion time is 40 μ sec maximum.

4.13 MN90228, MICRO NETWORKS COMPANY^{20,21}

The MN90228 is very similar to the MN5214 as described above in paragraph 4.11, except it was custom built to JPL specifications.

SECTION 5

RADIATION EFFECTS ON ADC SEMICONDUCTOR TECHNOLOGIES

A comparison of the various ADC semiconductor fabrication technologies to their radiation hardness in various radiation environments is given in Table 2 and Fig. 2. The radiation hardening of these technologies ranges from very soft to very hard and varies from environment to environment.

5.1 BI-MOS

Bi-MOS technology is a combination of I^2L and CMOS on the same chip for optimization of the analog and digital circuits and provides all the advantages of I^2L and radiation-hardened CMOS (when made with the radiation-hardened CMOS process).

5.2 BIPOLAR

The current bipolar technology is overall one of the most radiation-hard technologies for semiconductor devices. A number of ADC devices are currently available in bipolar technology.

5.3 CMOS

Standard CMOS (complementary metal oxide semiconductor) is a popular technology but it is radiation-soft. Many ADCs have been designed in CMOS.

5.4 CMOS-RAD HARD

Radiation-hardened CMOS processes are as hard as the hardest bipolar processes. Sandia Laboratory is using this radiation-hardened process for ADCs.

5.5 GaAs

GaAs may be a good technology for future devices. It is very hard in ionizing radiation environments but does suffer from bulk damage problems. Therefore, GaAs devices will not have the surface leakage problems of many bipolar devices but will have a sensitivity to electron, proton, neutron, and heavy ion damage, which is similar to the bipolar device sensitivity.

Except for speed, ADCs made of GaAs may not be any better than high-quality bipolar silicon devices.

Table 2. Comparative analysis of ADC semiconductor technologies

Technology	Speed	Total Dose, rad(Si)	Dose Rate, rad(Si)/sec	Neutron, n/cm ²	Single Event Upset (SEU)	Advantages	Disadvantages
BI-MOS (I ² L/CMOS)	Med	10 ⁶	10 ⁹	10 ¹³ -10 ¹⁴	Latches	Analog and Digital Optimized on Same Chip	Total dose hardness is dependent on CMOS
BIPOLAR	High	10 ⁴ -10 ⁶	10 ¹⁰	10 ¹⁴ -10 ¹⁵	Flips	High Speed, Stable Band Gap Voltage Ref.	Large Size, High Power
CMOS	Low	10 ³ -10 ⁵	10 ⁹	10 ¹⁵ -10 ¹⁶	Latches	Low Power, Small Size	Low Speed (Future CMOS will be faster)
CMOS (Rad Hard)	Low	10 ⁵ -10 ⁷	10 ⁹	10 ¹⁵ -10 ¹⁶	Latches	Low Power, Small Size	Low Speed (Future CMOS will be faster)
GaAs	High	>10 ⁷	>10 ¹⁰	10 ¹⁵	Flips	Highest Speed	Immature Technology, Expensive
I ² L	High	10 ⁴ -10 ⁶	10 ⁹	10 ¹³ -10 ¹⁴	Latches	High Speed, Small Size, Low Power	
NMOS	Low	10 ³ -10 ⁴	10 ⁸	10 ¹⁵ -10 ¹⁶	LOC/MOS Flips	Low Power, Small Size	Rad Soft, Low Speed
PMOS	Low	10 ³ -10 ⁴	10 ⁶	10 ¹⁵ -10 ¹⁶	-	Low Power, Small Size	Rad Soft, Low Speed
SOS/SOI	Med	10 ³ -10 ⁵	10 ¹⁰	10 ¹⁵ -10 ¹⁶	No Latch	Hard to Transient Radiation and Latchup	Expensive
SOS/SOI (Rad Hard)	Med	10 ⁵ -10 ⁷	10 ¹⁰	10 ¹⁵ -10 ¹⁶	No Latch	Hard to Transient Radiation and Latchup	Expensive

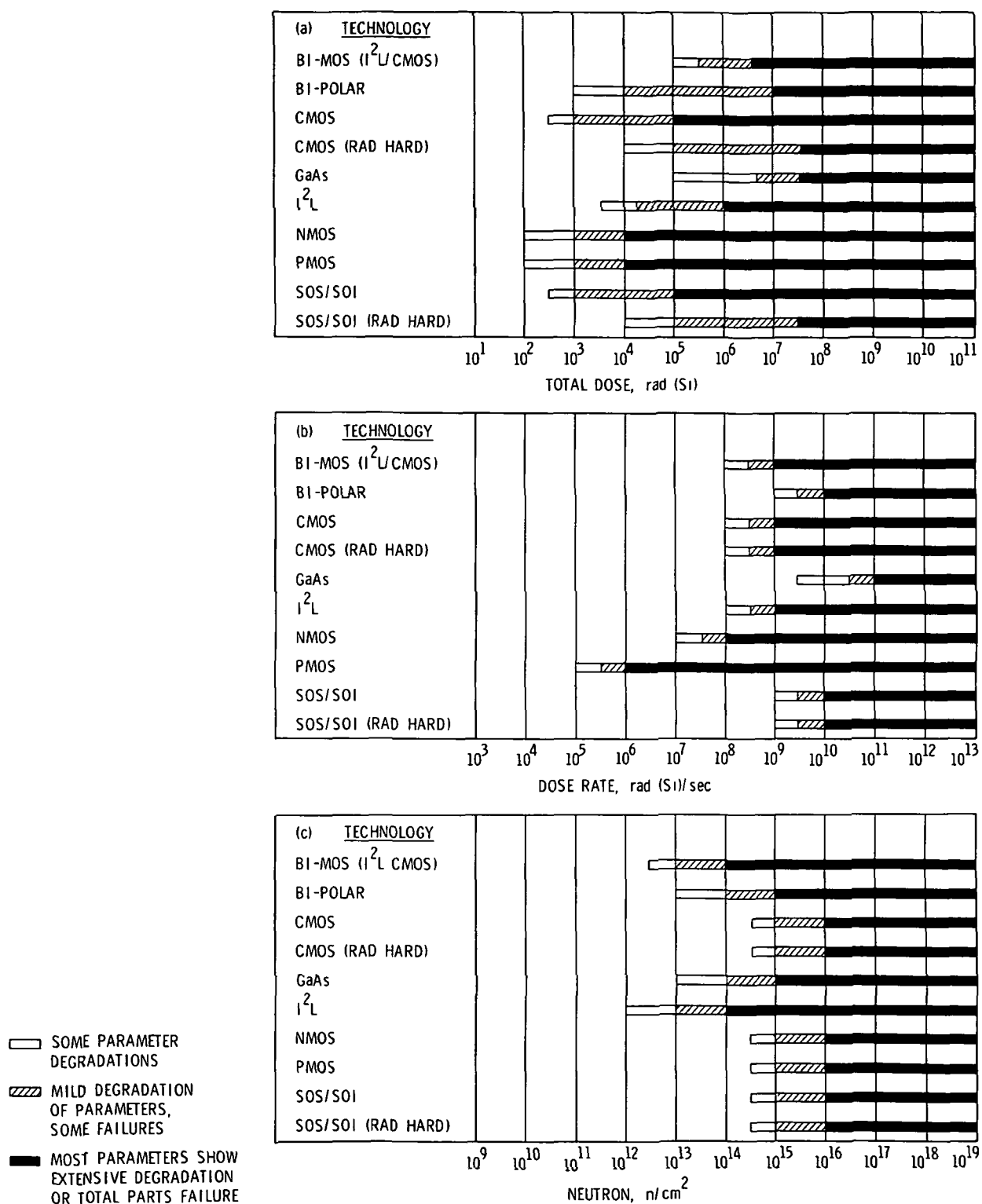


Figure 2. Radiation analysis of ADC semiconductor technologies:
 (a) total dose, (b) dose rate, and (c) neutron

5.6 I²L

I²L (integrated injection logic) is an overall radiation-hard technology incorporating high speed, small size, and low power.

5.7 NMOS

NMOS (N-type MOS) technology is very soft and shows little promise of being hardened.

5.8 PMOS

PMOS (P-type MOS) technology, like NMOS, is very soft and shows little promise of being hardened.

5.9 SOS AND SOI

SOS and SOI (silicon-on-sapphire and silicon-on-insulator) is soft to total dose but hard to other environments. Currently there is development work going on in the area of SOI, but little of it is directly related to ADCs.

5.10 SOI AND SOI-RAD HARD

Recent developments of radiation-hardened CMOS SOS and SOI have increased the total dose hardness to the same levels as radiation-hardened CMOS.

SECTION 6

ADC TEST DATA

For immediate needs in a radiation environment, there are a number of choices depending on the bit-resolution required by the system. Table 3 lists all ADCs tested by JPL to date.

8-bit: For 8-bit applications, the AMD AM6108 and AM6148 should be considered. Radiation tests of these devices indicate that they are hard to at least 600 krad(Si). This device family has also been neutron tested to 1×10^{13} n/cm² with little parameter degradation.

10-bit: Those with applications requiring a 10-bit ADC should consider the ADI AD571, which has been radiation tested and is hard to at least 75 krad(Si), although the latest date codes (1981) tested indicated the devices were hard to 300 krad(Si).

12-bit: Designers requiring a 12-bit ADC should consider the AD574-MONO or the AM6112. The AD574-MONO is a new monolithic design of the old AD574, and has a radiation hardness of at least 1 Mrad(Si).

The AM6112 has been neutron tested to 1×10^{13} n/cm² with little degradation. In total dose the device is hard to at least 600 krad(Si).

16-bit: When a 16-bit ADC is required, consideration should be given to the Micro Networks MN5290. This device has been radiation tested and is hard to at least 1 Mrad(Si).

Table 3. ADCs tested by JPL

Part No.	Date Code	Mfg	Process	Bits	Power, mW	Speed, μ s	Total Dose krad(Si)	Neutron, n/cm ²	Remarks†
TDC1021J	7935	TRW	Bipolar	4	400	0.4	>600		Flash
AM6108	8237DM	AMD	Bipolar	8	600	0.5	300		
AM6108	8413FM	AMD	Bipolar	8	600	0.5		>1E13	
AM6148	8220D	AMD	Bipolar	8	600	0.9	600		
AM6148	8405DP	AMD	Bipolar	8	600	0.9	1000		
TDC1001J	7802C	TRW	Bipolar	8	400	0.4	>2500		
AD571	78461V	ADI	Bipolar	10	400	25	75		
AD571	78461V	ADI	Bipolar	10	400	25	150		
AD571	7922	ADI	Bipolar	10	400	25	75		
AD571	R&D(80)	ADI	Bipolar	10	400	25	75		
AD571	8105	ADI	Bipolar	10	400	25	300		
AD571	8107	ADI	Bipolar	10	400	25	300		
AD571	8110	ADI	Bipolar	10	400	25	300		
AD573	8425	ADI	Bipolar	10	350	15	75		
AD573	8425	ADI	Bipolar	10	350	15	75*		
AD573	8428	ADI	Bipolar	10	350	15	30		
AD573	8428	ADI	Bipolar	10	350	15	75*		
AD7570	7844	ADI	CMOS	10	40	40	15		
MP7570	7803	MPS	CMOS	10	40	40	20		
AD574	7903N	ADI	Bipolar	12	400	25	30		} 3 chip hybrids
AD574	7905N	ADI	Bipolar	12	400	25	30		
AD574	7909N	ADI	Bipolar	12	400	25	30		
AD574A	250	ADI	Bipolar	12	400	25	150		} 2 chip hybrids
AD574A	8430	ADI	Bipolar	12	400	25	30	<3.3E12	
AD574-MONO (1985)		ADI	Bipolar	12	400	25	>1000		
ADC1210	7840	NSC	CMOS	12	135	100	20		
AM6112	8251D	AMD	Bipolar	12	600	3.0	1000		
AM6112	8410DP	AMD	Bipolar	12	600	3.0	600		
AM6112	8426EM	AMD	Bipolar	12	600	3.0		>1E13	
HI574	8437	HAR	CMOS/ Bipolar	12	135	25	10		Hybrid
HI674A	8422	HAR	CMOS/ Bipolar	12	135	15	10		Hybrid
MN5211	8102	MNC	Bipolar	12	600	3.0	>600		Hybrid
MN5214	8102	MNC	Bipolar	12	600	3.0	30		Hybrid
MN5216	7909	MNC	Bipolar	12	600	3.0	150		Hybrid
MN5216	7910	MNC	Bipolar	12	600	3.0	150		Hybrid
MN90228	8141	MNC	Bipolar	12	600	3.0	>600		Same as MN5214

†Unless otherwise noted, each is a monolithic chip.

*These devices were radiation tested using Co-60 gamma rays; all other devices were tested using the Dynamitron, 2.5 MeV electrons, as the radiation source.

Table 3. ADCs tested by JPL (Continued)

Part No.	Date Code	Mfg	Process	Bits	Power, mW	Speed, μ s	Total Dose krad(Si)	Neutron, n/cm ²	Remarks [†]
MN90228	8141	MNC	Bipolar	12	600	3.0	600		Hybrid
MP574	(85x)	MPS	CMOS/ Bipolar	12	135	25	50		Hybrid
MN5290	8419	MNC	Bipolar	16	830	35	>1000		Hybrid

[†]Unless otherwise noted, each is a monolithic chip.

SECTION 7

CONCLUSIONS AND RECOMMENDATIONS

7.1 CONCLUSIONS

The objectives of this study have been met with new analog to digital converters complying with space and/or strategic weapon requirements being developed. Bit configuration and operating speed have been improved and configurations with optimized special features to ease equipment design and operation are being developed. Current and potential technologies are being evaluated and processes are being developed to optimize performance and comply with space and/or strategic radiation hardening requirements. It is intended that these devices will be suitable for a wide range of equipment and systems applications.

ADC development is evolving in two directions: (1) the standard monolithic ADC, and (2) the monolithic ADC with extended features, which includes the ability to interface directly with the microprocessor bus. This second type will eventually evolve into the "smart ADC," which will have various microprocessor functions (RAM, ROM, etc.) on the chip.

There are individual applications best served by each type of ADC chip but both types are being developed and have been monitored during this study. The primary concern for the immediate future is the monolithic ADC, but this study has not overlooked the requirements for, and development of, the "smart ADC."

7.2 RECOMMENDATIONS

Application and design engineers with immediate needs now have several choices of ADCs which may meet their requirements. The AMD AM6108 and AM6148 should be considered for 8-bit applications, the ADI AD571 for 10-bit applications, the ADI AD574-MONO and AMD AM6112 for 12-bit applications, and the Micro Networks MN5290 for 16-bit applications. These are all monolithic devices except for the MN5290 and are hard to at least 300 krad(Si). Increased hardness may be obtained on these devices by "tweaking" the manufacturing process. With vendor cooperation, process variations may be made that will improve the typical hardness of the devices by a factor of two to four times.

To continue the development of radiation hardened ADCs, it is recommended that:

- (1) Meetings, conferences, and workshops be conducted on radiation hardening of ADCs, in order to define relevant research and establish communications between cooperating laboratories, researchers and industry;
- (2) Further development of faster radiation hardened ADCs, which have higher bit resolution, use less power and include additional functional elements such as microprocessor control, on-board RAM and ROM, and internal programmability, should be encouraged.

- (3) ADC designers should be encouraged to apply radiation hardening techniques, whenever cost effective, during new ADC development, redesign, or when process changes are made;
- (4) Radiation tests of candidate ADC devices as well as new designs, processes, and technologies be continued; and
- (5) The interface between ADC users and manufacturers be continued and increased.

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